COURSE OBJECTIVE:

Field Programmable Gate Arrays (FPGA) and Application Specific Integrated Circuits (ASIC) are both used to implement VLSI logics, but they serve different purposes and suit different stages of product development. FPGAs are reconfigurable devices that allow designers to implement and test hardware functionality, making them good for research, prototyping, and low-volume makes. They offer flexibility and shorter time-to-market but come with higher per-unit costs and lower performance compared to ASICs, which on the other hand, are custom-manufactured chips optimized for specific tasks, offering superior performance, lower power consumption, and reduced unit cost in high-volume production. However, ASIC development involves a complex and costly design flow, making it suitable for mature designs with stable requirements. Part 2 of this course would majorly focus on the Static time analysis, digital designs, Verilog coding Implementation in FPGAs and Single stage MOS Amplifiers designs. There will be expert lectures from renowned Professor of IITs and other eminent Institutes. The course would also give an idea on basic ASIC designs flow and single stage amplifier design using Tanner EDA Tools.

COURSE HIGHLIGHTS:

- Advanced concepts in VLSI design.
- Recent advances in VLSI technologies.
- Design of ADC and DACs.
- Static Time Analysis.
- Introduction to Single Stage Amplifier Design and stability analysis.
- Digital Design Using Verilog HDL and Implementation in FPGAs.
- Analog Design Using Tanner EDA Tools.
- Introduction to Layout.

Major Topics to be Covered:

- ❑ Introduction to Complete VLSI Design Flow
- ❑ Reconfigurable VLSI Design using FPGA
- ❑ HDL languages: Verilog in Vivado
- ❑ Synthesis and implementation flow
- ❑ Concept of FPGA vs ASIC design Implementation
- ❑ Tanner Tools in ASIC Flow
- ❑ Design and layout of MOS transistors
- ❑ Single Stage MOS amplifiers.
- ❑ Introduction to Operational Trans-conductance Amplifier (OTA) design.
- ❑ Concept of Stability, Gain Margin and Phase Margin of OTA.

Technically co-sponsored by IEEE Rourkela Sub-Section

Student's Workshop & Faculty Development Program on

FPGA to ASIC – A Complete VLSI Design Flow

(Part 2: Static Time Analysis and Amplifier Design)

30th January to 3rd February 2026

in ONLINE MODE

Coordinators:
Dr. Santanu Sarkar
Dr. Atin Mukherjee
&
Dr. Ayaskanta Swain

Dept. of Electronics & Communication Engg.
National Institute of Technology Rourkela
Rourkela – 769 008, Odisha, India

Technically Co-sponsored by:

IEEE ROURKELA SUBSECTION

ABOUT NIT ROURKELA:

National Institute of Technology (NIT) Rourkela was founded as Regional Engineering College, Rourkela in 1961. It is a prestigious Institute with a reputation for excellence at both undergraduate and postgraduate levels, fostering the spirit of national integration among the students, a close interaction with industry and a strong emphasis on research, both basic and applied. It's been consistently ranked within top 20 engineering institutes for 10 consecutive years as per MHRD's NIRF, Govt. of India.

The city of Rourkela is a bustling industrial town, cosmopolitan by nature and is well connected to all parts of the country by road and rail. It is en-route Howrah-Mumbai main line of South-Eastern Railway. Nesting amidst greenery on all sides, NIT campus is approximately 7km from Rourkela railway station. The nearby airports are Jharsuguda, Ranchi, Kolkata and Bhubaneswar.

Website: www.nitrkl.ac.in

ABOUT DEPARTMENT OF ECE:

The mission of the Department of ECE, NIT Rourkela, is to advance and spread knowledge in the area of communication, instrumentation, signal processing and VLSI leading to creation of wealth and welfare of humanity. Vision of this department is to become a nationally acclaimed department of higher learning that will serve as a source of knowledge and expertise for the society. In this department, two undergraduate and five post graduate courses are running at present. Faculty members of the department are involved with research work in various domains: VLSI Design & Embedded systems, Signal & Image Processing, RF and Microwave Systems, Communication & Networks, and Electronics & Instrumentation Engineering.

NIRF Ranking - 2025

13	07	30	34
Engineering	Architecture	Research	Overall

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REGISTRATION DETAILS

Registration is open to UG and PG students & Faculty members of Electronics and Electrical Engineering, Sciences, Physics, Mathematics, Post Doctoral Fellows, Research Scholars. Complete Registration through (after payment): **https://forms.gle/zzeWCuVAZHPUzVwU6**

Last Date of Registration:
10th January 2026

Registration Type	Fees (*Non Refundable*)
Faculty / Lab Staff	**₹ 749** (including GST)
Students(RS/PG/UG)	**₹ 499** (including GST)
R&D/Industry People	**₹ 999** (including GST)

MODE OF PAYMENT: (Online only)

Transfer the Fee amount using UPI or NEFT: (mention in remarks as: **ANRF ASIC**)

UPI ID: 01389517841@sbi

NEFT Account details:

Acct. No.: **10138951784**
Name: **CONTINUING EDUCATION NIT ROURKELA**
Bank: State Bank of India
Branch: NIT Rourkela Campus
IFS Code: **SBIN0002109**

Attach the payment receipt in the google form for registration (link mentioned above).

Certificates will be given only to those participants who will attend at least 90% of sessions of the course.