COURSE OBJECTIVE:

Field Programmable Gate Arrays (FPGA) and Application Specific Integrated Circuits (ASIC) are both used to implement VLSI logics, but they serve different purposes and suit different stages of product development. FPGAs are reconfigurable devices that allow designers to implement and test hardware functionality, making them good for research, prototyping, and low-volume makes. They offer flexibility and shorter time-to-market but come with higher per-unit costs and lower performance compared to ASICs, which on the other hand, are custom-manufactured chips optimized for specific tasks, offering superior performance, lower power consumption, and reduced unit cost in high-volume production. However, ASIC development involves a complex and costly design flow, making it suitable for mature designs with stable requirements. Part 1 of this course would majorly focus on the Digital designs, Verilog codings & implementation in FPGAs. FPGA being popular in space technologies in recent days, it has become important to make them more robust and capable of working in harsh environment increasing the need of defect tolerance. The course would also give an idea on basic ASIC designs using Tanner EDA Tools.

अनुसंधान नेशनल रिसर्च फाउंडेशन
Anusandhan National Research Foundation

COURSE HIGHLIGHTS:

- Foundational concepts in VLSI design.
- Recent advances in VLSI technologies.
- Design of FPGAs using CLBs, LUTs, flip-flops and routing.
- VLSI designs for signal processing applications.
- Introduction to defect tolerance and reliability.
- FPGAs in defect tolerant system design.
- Digital Design Using Verilog HDL and implementation in FPGAs.
- Analog Design Using Tanner EDA Tools.

MAJOR TOPICS TO BE COVERED:

- Complete Modern VLSI Design Flow
- Reconfigurable VLSI Design
- Architecture of FPGAs
- Defect Tolerance in FPGAs
- FPGAs in Healthcare
- HDL languages: Verilog in Vivado
- Synthesis and implementation flow
- FPGA vs ASIC design
- Tanner Tools in ASIC Flow

ANRF (erstwhile SERB) Sponsored

Five Days Student Workshop and Faculty Development Program on

FPGA to ASIC – A Complete VLSI Design Flow

(Part 1: FPGAs in Defect Tolerance)

06th January to 10th January 2026

in ONLINE MODE

Coordinators:

Dr. Atin Mukherjee
Dr. Santanu Sarkar

Co-coordinator:
Prof. Santanu K. Behera

Dept. of Electronics & Communication Engg.
National Institute of Technology Rourkela
Rourkela – 769 008, Odisha, India

Technically Co-sponsored by:

IEEE ROURKELA SUBSECTION

ABOUT NIT ROURKELA:

National Institute of Technology Rourkela is a prestigious Institute with a reputation for excellence at both undergraduate and postgraduate levels, fostering the spirit of national integration among the students, a close interaction with industry and a strong emphasis on research, both basic and applied.

34 NIRF Overall	13 NIRF Engineering	30 NIRF Research	281-290 QS Asia

ABOUT DEPARTMENT OF ECE:

There are two undergraduate, and five post graduate courses are running in the ECE department of NIT Rourkela. Faculty members of the department are involved with research work in various domains: VLSI Design & Embedded systems, Signal & Image Processing, RF and Microwave Systems, Communication & Networks, and Electronics & Instrumentation Engineering.

WHO CAN ATTEND:

This workshop is open to the UG/ PG Students, Research Scholars (RS), Post-doctoral Fellows, Faculty Members, Laboratory Technicians, Industry and R&D Personnel etc. in all disciplines of Engineering and Sciences.

Last Date of Registration:
10th December 2025

FEES:

Registration Type	Fees (*Non Refundable*)
Faculty / Post-doct.	**NIL**
Students(RS/PG/UG)	**₹ 295** (₹250 + GST)
R&D/Industry People	**₹ 885** (₹750 + GST)
Technical Staff etc.	**₹ 885** (₹750 + GST)
NITR Staff/ Student	**NIL**

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REGISTRATION DETAILS

Complete Registration through (after payment):
https://forms.gle/4mUenaxCUoifY9c98

MODE OF PAYMENT: (Online only)

Transfer the Fee amount using UPI or NEFT:
(mention in remarks as: **ANRF FPGA**)

UPI Details:

01389517841@sbi

NEFT Account details:

Acct. No.: **10138951784**
Name: **CONTINUING EDUCATION NIT ROURKELA**
Bank: State Bank of India
Branch: NIT Rourkela Campus
IFS Code: **SBIN0002109**

Mention payment remarks as: **ANRF FPGA**
Attach the payment receipt in the google form for registration (link/ QR mentioned above)

Certificates will be given only to those participants who will attend all sessions of the course.