Atin Mukherjee

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National Institute of Technology Rourkela, Rourkela – 769008, Odisha, India
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Academics

- **Ph.D.**, Electronics and Electrical Communication Engineering, *Indian Institute of Technology, Kharagpur*.

Dissertation: Fault Tolerant VLSI Architecture Design for Real-Time Signal Processing Applications.
Thesis submitted on 31st December, **2015**; **Defended** on 06th July, **2017**; **Awarded** on 06th August, **2017.**

- **Master of Technology (M. Tech.)**, Electronics and Electrical Communication Engineering, *IIT Kharagpur*.

CGPA: 9.67/10, **Stream**: Visual Information and Embedded Systems Engineering, Year: **2011**.

- **Bachelor of Engineering (B. E.)**, Electronics and Telecommunication Engineering, *Jadavpur University*.

CGPA: 9.35/10, Year: **2009**.

- Passed **(10 + 2)** with **93.4%** under *West Bengal Council of Higher Secondary Education* in **2005**.

Research Areas

- **Digital VLSI structure and optimization**
- **Fault tolerant VLSI architecture**
- **VLSI testing and hardware verification**
- **Radiation hardened memory design**
- **On-chip ECG processing and classification**
- **Low power memory design**
- **Low-cost video processor for HEVC coding**

Ph.D. Dissertation

Title: Fault Tolerant VLSI Architecture Design for Real-Time Signal Processing Applications

Abstract: Fault tolerance has become extremely important in today's digital design because of the high failure rates of chips due to the increase in the design complexities and the density of transistors in them. We have identified the major pitfalls of the existing fault tolerant methods and tried to rectify them as far as possible. We have modified the traditional dynamic reconfiguration method and make it suitable for real-time signal processing applications incorporating hot-standby, graceful degradation, cascadability and *C*-testability to it. We have also proposed some new static redundancy techniques, which are superior to the existing methods in various aspects and also have practical applicability.

- *RTL design, simulation & verification by using verilog HDL and schematic level in XILINX with virtex-6*
- *Design and verification along with calculation of area and critical path results using SYNOPSYS tools*
- *Area and delay verifications using CADENCE tools.*
- *Work on real-time signal processing application like video processor.*

M.Tech. Thesis

Title: VLSI Architecture Design of a Fault Tolerant Motion Estimation Block with Graceful Degradation

Summary: We designed the VLSI architecture for hexagon based motion estimation unit and made it fault tolerant using various existing and newly proposed fault tolerant approaches, thus increasing the reliability of the whole video processor.

- *MATLAB implementation of the algorithms.*
- *RTL design, simulation & verification using Verilog HDL and schematic level in XILINX with virtex-4 kit.*

Term Project (M.Tech.)

Title: Testing and Verification for Embedded Systems

- *Studied on different types of software testing and basic concepts of SoCs and NoCs.*
- *Learned System C.*
- *Implemented Traffic Light Controller using ARM (Keil MCB2100 Microcontroller Board).*
- *Injected faults in the system and run BIST to identify them.*

B.E. Project

Title: Design of CMOS Class-E Radio Frequency Power Amplifier

Summary: We designed an efficient 950MHz fully differential power amplifier for wireless communications in standard 0.18µm CMOS technology. The power amplifier employed a fully differential class-E topology to achieve high power efficiency by exploiting its soft-switching property.

- *Simulation of circuits in Virtuoso Schematic Composer by Cadence for AMS 180nm CMOS technology.*

Work Experience

- **Assistant Professor**, Department of Electronics and Communication Engineering, *National Institute of Technology Rourkela* since March 2018.
- **Assistant Professor**, Department of Electronics and Communication Engineering, *Techno India University (TIU)*, *Kolkata*, from January 2016 to March 2018.

Courses Taught

- Integrated Circuit for Digital Signal Processing
- Testing and Verification of VLSI Circuits
- Microprocessors
- Semiconductor Devices
- Embedded Systems
- Digital VLSI Design
- Basic Electronics Laboratory
- Digital Electronics and HDL Laboratory
- Microprocessor Laboratory
- Reconfigurable System Design Laboratory
- Embedded Design Laboratory
- VLSI Design Laboratory

Sponsored Project

Principle Investigator (PI) of project on *Development of complete resilient reconfigurable field programmable gate array (FPGA) with defect tolerant controller for payload designs in nano-satellites.*

Budget: 30.57 lakhs Duration: 3 years Sponsor: DST-ANRF (erstwhile SERB)

Reviewer

- IEEE Transactions on Very Large Scale Integration (*VLSI*) Systems
- IEEE Transactions on Circuits and Systems I
- IEEE Transactions on Circuits and Systems II: Express Briefs
- Elsevier Microelectronics Reliability
- Elsevier Microelectronics Journal
- IET Circuits, Devices and Systems *and many more*

Achievements

- Received *Best paper award* in National Conference on Intelligent Systems, IoT, and Wireless Communication for the Society (IIWCS) 2024.
- Best paper award in 13th Inter-University Engineering, Science & Technology Academic Meet – 2023 (National Conference) by Forum of Scientists, Engineers & Technologists (FOSET), April 2023, Kolkata.
- Quarter finalist in Swadeshi Microprocessor Challenge 2020.
- Received *Faculty Advisor Appreciation Award* by ICS, NIT Rourkela for 2018 BTech EI batch.
- Received *Best paper award* in International Conference on Computer, Electrical & Communication Engineering (ICCECE) 2017.
- Certificate for attending FDP organized by IIT Kharagpur at Techno India University, Kolkata, April 2016
- MHRD Fellowship for pursuing PhD and M. Tech. at IIT Kharagpur
- Ranked 218 in GATE 2009 (Percentile: 99.47)
- Ranked 40 in West Bengal Joint Entrance Examination 2005 (W.B.J.E.E. ’05)
- Ranked 1st in Science Talent Search Examination (Indian science congress association) in 2000 and 2001
- Ranked 1st in Achievement-cum-Diagnostic test in Mathematics in 1998-’99 and 1999-2000
- Scholarship for clearing Britti (primary final examination) in 1996-’97

Administrative Work

- Teacher-in-Charge of the ECE Dept. in Techno India University from Jan 2017 to Mar 2018
- PIC-UG/PG Project, NIT Rourkela (July 2018-June 2020)
- Faculty advisor of the 2018-2022 BTech-EI students, NIT Rourkela
- Faculty advisor of the 2022-2024 MTech-VLSI students, NIT Rourkela
- PIC of computer simulation laboratory (July 2020 to June 2023), NIT Rourkela
- PIC-Imprest money, NIT Rourkela (July 2019 to June 2023)
- Member of departmental purchase committee (July 2019 to June 2023)
- Member of institute website committee (July 2022 to June 2023), NIT Rourkela
- Treasurer, IEEE Consumer Technology Society Chapter, IEEE Bhubaneswar Section (Jan 2023 to Dec 2024)
- PIC-departmental student societies and activities (since July 2023)
- Departmental chairman for Accreditation and Ranking (since July 2023)
- Spoke person of the institutional Pradhan Mantri Kaushal Vikas Yojana (PMKVY) program (since July 2023)
- Vice-Chair Website, IEEE Rourkela Subsection (Since Jan 2024)
- Institutional Capacity Building on Design & Entrepreneurship (CBDE) program member (since July 2024)

List of Publications

In Journals

1. S. Kumar and A. Mukherjee, “Design of Robust SRAM Cell With Enhanced Soft-Error Hardening for Radiation-Prone Applications,” IEEE Transactions on Device and Materials Reliability, doi: 10.1109/TDMR.2025.3609912. (Early Access)
2. A. Gon and **A. Mukherjee**, “Design of a low-area hardware architecture to predict early signs of sudden cardiac arrests”, *Elsevier Microprocessors and Microsystems,* vol. 109, no. 105082, pp. 1-11, Sep. 2024. DOI: 10.1016/j.micpro.2024.105082.
3. S. Kumar and **A. Mukherjee**, “Low Cost and High Performance Double-node Upset Resilient Latch for Low Orbit Space Applications,” *Wiley International Journal Of Circuit Theory and Applications*, vol. 52, no.5, pp. 2534-2549, May 2024. DOI: 10.1002/cta.3855.
4. A. Panigrahi, H. Sharma, and **A. Mukherjee**, “Video-based HR Measurement Using Adaptive Facial Regions with Multiple Color Spaces,” *Elsevier Biocybernetics and Biomedical Engineering*, vol. 44, no. 1, pp. 68-82, Jan.-Mar. 2024, DOI: 10.1016/j.bbe.2023.12.001.
5. A. Gon and **A. Mukherjee**, “Design of Hardware-efficient PVC Recognition and Classification System for Early Detection of Sudden Cardiac Arrests,” *AEU - International Journal of Electronics and Communications (Elsevier)*, vol. 172, no. 154955, pp. 1-13, Dec. 2023. DOI: 10.1016/j.aeue.2023.154955.
6. S. Kumar and **A. Mukherjee**, “High Performance Radiation-hardened SRAM Cell Design for Robust Applications,” *Elsevier Microelectronics Journal*, vol. 140, no. 105934, pp. 1-12, Oct. 2023. DOI: 10.1016/j.mejo.2023.105934.
7. S. Kumar and **A. Mukherjee**, “Design of Soft-Error Resilient SRAM Cell with High Read and Write Stability for Robust Operations,” *AEU - International Journal of Electronics and Communications (Elsevier)*, vol. 168, no. 154719, pp. 1-10, Aug. 2023. DOI: 10.1016/j.aeue.2023.154719.
8. Md B. Arshad and **A. Mukherjee**, “Comparative Analysis of Deep Learning Models for the Detection of Epileptic Seizure,” *American Journal of Advanced Computing,* vol. 2, no. 1, pp. 29-35, Apr. 2023. DOI: 10.15864/ajac.21016.
9. A. Gon and **A. Mukherjee**, “FPGA-Based Low-Cost Architecture for R-Peak Detection and Heart-Rate Calculation Using Lifting-Based Discrete Wavelet Transform,” *Springer Circuits, Systems, and Signal Processing*, vol. 42, no. 1, pp. 580-600, Jan. 2023. DOI: 10.1007/s00034-022-02148-7.
10. S. Kumar and **A. Mukherjee**, “A Triple-Node Upset Self-Healing Latch for High Speed and Robust Operation in Radiation-Prone Harsh-Environment,” *Elsevier Microelectronics Reliability*, vol. 139, no. 114857, pp. 1-12, Dec. 2022. DOI: 10.1016/j.microrel.2022.114857.

11. S. Kumar and **A. Mukherjee**, "A Highly Robust and Low-Power Real-Time Double Node Upset Self-Healing Latch for Radiation-Prone Applications," *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems*, vol. 29, no. 12, pp. 2076-2085, Dec. 2021. DOI: 10.1109/TVLSI.2021.3110135.

12. **A. Mukherjee** and A. S. Dhar, "Triple Transistor Based Triple Modular Redundancy with Embedded Voter Circuit," *Elsevier Microelectronics Journal*, vol. 87, pp. 101-109, May 2019. DOI: 10.1016/j.mejo.2019.03.014.

13. **A. Mukherjee** and A. S. Dhar, "Reliable VLSI Architecture Design Using Modulo-Quad-Transistor Redundancy Method," *Springer Circuits, Systems, and Signal Processing*, vol. 37, no. 5, pp. 5595–5615, May 2018. DOI: 10.1007/s00034-018-0837-1.

14. S. Banerjee, E. Sarkar, and **A. Mukherjee**, "Effect of Fin Width and Fin Height on Threshold Voltage for Triple Gate Rectangular FinFET," *TIU Transactions on Intelligent Computing,* vol. 2, pp. 27-30, June 2018.

15. **A. Mukherjee** and A. S. Dhar, "Triple Transistor Based Fault Tolerance for Resource Constrained Applications," *Elsevier Microelectronics Journal*, vol. 68, pp. 1-6, Oct. 2017. DOI: 10.1016/j.mejo.2017.08.005.

16. **A. Mukherjee** and A. S. Dhar, "Choice of Granularity for Reliable Circuit Design Using Dynamic Reconfiguration," *Elsevier Microelectronics Reliability*, vol. 63, pp. 291-303, Aug. 2016. DOI: 10.1016/j.microrel.2016.04.001.

17. **A. Mukherjee** and A. S. Dhar, "Fault Tolerant Architecture Design Using Quad-Gate-Transistor Redundancy," *IET Circuits, Devices and Systems*, vol. 9, no. 3, pp. 152-160, May 2015. DOI: 10.1049/iet-cds.2014.0106.

18. **A. Mukherjee** and A. S. Dhar, "Real-Time Fault-Tolerance with Hot-Standby Topology for Conditional Sum Adder," *Elsevier Microelectronics Reliability*, vol. 55, no. 3-4, pp. 704-712, Feb.-Mar. 2015. DOI: 10.1016/j.microrel.2014.12.011.

List of Publications

In Conferences

1. S. Rakh, A. Gon, H. Sharma, and **A. Mukherjee**, “Optimized ECG Analysis for Atrial Fibrillation Detection: A Lifting-Based Wavelet Approach.” 16th IEEE International Conference on Computing, Communication and Networking Technologies (*ICCCNT*), IIT Indore, India, 2025. (Accepted)
2. A. K. Nayak and **A. Mukherjee**, “Hardware-Specific Implementation of Neural Network for Handwritten Digit Detection,” in Recent Trends in Intelligent Systems and Next Generation Wireless Communication, Proceedings of IIWCS 2024, Springer Lecture Notes in Networks and Systems (LNNS), Singapore, vol. 1329, Aug. 2025, pp. 203-214, DOI: 10.1007/978-981-96-4741-5_18.
3. A. Panigrahi, H. Sharma and **A. Mukherjee**, “Investigation on different color spaces for non-contact heart rate monitoring using facial videos," 7th International Conference on Signal Processing, Computing and Control (ISPCC), SOLAN, India, Mar. 2025, pp. 869-873, DOI: 10.1109/ISPCC66872.2025.11039565.
4. S. Paryani and **A. Mukherjee**, “Implementation of HEVC: Residual Image-Free Compression Approach,” IEEE International Conference on Smart Power Control and Renewable Energy (*ICSPCRE*), NIT Rourkela, India, Jul. 2024, pp. 1-6, DOI: 10.1109/ICSPCRE62303.2024.10675003.
5. V. K. Verma and **A. Mukherjee**, “Design of Multi-bit Fault Tolerant Array Multiplier,” IEEE International Conference on Electronics, Computing and Communication Technologies (*CONECCT*), IISc Bangalore, India, Jul. 2024, pp. 1-6, DOI: 10.1109/CONECCT62155.2024.10677061.
6. A. Panigrahi, H. Sharma and **A. Mukherjee**, “Non-contact heart rate extraction from facial RGB videos using alternate color spaces: a comparison study,” National Conference on Intelligent Electronic Systems and Applications (NCIESA), NIT Kurukshetra, India, Feb. 2024, pp. 1-5.
7. A. Panigrahi, A. K. Sharma, H. Sharma and **A. Mukherjee,** “Contactless HR Measurement from Facial Videos Using Alternative Color Spaces with CEEMDAN,” IEEE International Conference on Signal Processing and Communication (*ICSC*), Noida, India, Dec. 2023, pp. 522-527. DOI: 10.1109/ICSC60394.2023.10441625.
8. K. Sahu and **A. Mukherjee**, “Design of a Self-reconfigurable Incrementer for Fault Tolerant VLSI Architecture,” IEEE Silchar Subsection Conference *(SILCON)*, NIT Silchar, India, Nov. 2023, pp. 1-5. DOI: 10.1109/SILCON59133.2023.10405199.
9. A. K. Samal, S. Kumar and **A. Mukherjee**, “Design of Single Node Upset Resilient Latch for Low Power, Low Cost and Highly Robust Applications,” IEEE International Test Conference in Asia *(ITC-Asia)*, Matsue, Japan, Sep. 2023, pp. 1-5. DOI: 10.1109/ITC-Asia58802.2023.10301176.

10. S. M. Satute, D. Divakar, Ambili V. and **A. Mukherjee**, "Design of a High-Speed Floating-Point Multiplier," International Conference on Low-Energy Digital Devices and Computing (ICLED), NUS Department of Architecture, Singapore, Jun-Jul. 2023 *[Abstract presentation]*.

11. A. Gon and **A. Mukherjee**, "Design and FPGA Implementation of an Efficient Architecture for Noise Removal in ECG Signals Using Lifting-Based Wavelet Denoising," IEEE 11th International Symposium on Electronic Systems Devices and Computing *(ESDC)*, IIIT Sri City, India, May 2023, pp. 1-6. DOI: 10.1109/ESDC56251.2023.10149865.

12. **A. Mukherjee**, "VLSI Architecture Design of Motion Estimation Block with Hexagon-Diamond Search Pattern for Real-Time Video Processing," IEEE 18th India Council International Conference (*INDICON*), IIT Guwahati, India, Dec. 2021, pp. 1-6. DOI: 10.1109/INDICON52576.2021.9691531.

13. S. Kumar and **A. Mukherjee**, "A Self-Healing, High Performance and Low-Cost Radiation Hardened Latch Design," IEEE 34th International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (*DFT*), Athens, Greece, Oct. 2021, pp. 1-6. DOI: 10.1109/DFT52944.2021.9568359.

14. A. R, D. Chaudhary and **A. Mukherjee**, "Design of Low-Power DDR Controller and DRAM for Deep Learning and Server Applications," IEEE International Conference on Computing, Power and Communication Technologies (*GUCON*), University of Malaya, Kuala Lumpur, Malaysia, Sept. 2021, pp. 1-6. DOI: 10.1109/GUCON50781.2021.9573889.

15. S. Pal and **A. Mukherjee**, "A New Power-Gated Hybrid Defect Tolerant Approach Based on Modular Redundancy," IEEE Asian Conference on Innovation in Technology (*ASIANCON*), Pune, India, Aug. 2021, pp. 1-4. DOI: 10.1109/ASIANCON51346.2021.9544937.

16. **A. Mukherjee**, "Defect Tolerant Approach for Reliable Majority Voter Design Using Quadded Transistor Logic," IEEE REGION 10 CONFERENCE (*TENCON*), Osaka, Japan, Nov. 2020, pp. 165-169. DOI: 10.1109/TENCON50793.2020.9293826.

17. A. Gon and **A. Mukherjee**, "Removal of Noises from an ECG Signal Using an Adaptive S-Median Thresholding Technique," IEEE Applied Signal Processing Conference (*ASPCON*), Kolkata, India, Oct. 2020, pp. 89-93. DOI: 10.1109/ASPCON49795.2020.9276706.

18. D. Chaudhary, V. Muppalla and **A. Mukherjee**, "Design of Low Power Stacked Inverter Based SRAM Cell with Improved Write Ability," IEEE Region 10 Symposium (*TENSYMP*), Dhaka, Bangladesh, Jun. 2020, pp. 925-928. DOI: 10.1109/TENSYMP50017.2020.9230809.

19. **A. Mukherjee** and A. S. Dhar, "Defect Tolerant Majority Voter Design Using Triple Transistor Redundancy," IEEE International Symposium on Smart Electronic Systems (*iSES*) (Formerly iNiS), NIT Rourkela, India, Dec. 2019, pp. 63-68. DOI: 10.1109/iSES47678.2019.00026.

20. P. Das, A. Sinha and **A. Mukherjee**, "Fault Tolerant Architecture Design of a 4-bit Magnitude Comparator," IEEE International Conference on Computer, Electrical & Communication Engineering (*ICCECE*), Kolkata, India, Dec. 2017, pp. 1-6. DOI: 10.1109/ICCECE.2017.8526235.

21. **A. Mukherjee** and A. S. Dhar, “New Triple-Transistor Based Defect-Tolerant Systems for Reliable Digital Architectures,” IEEE International Symposium on Circuits and Systems (*ISCAS*), Lisbon, Portugal, May 2015, pp. 1917-1920. DOI: 10.1109/ISCAS.2015.7169047.
22. **A. Mukherjee** and A. S. Dhar, “Double-Fault Tolerant Architecture Design for Digital Adder,” IEEE Students' Technology Symposium (*TechSym*), IIT Kharagpur, India, Feb.-Mar. 2014, pp. 154-158. DOI: 10.1109/TechSym.2014.6807932.
23. **A. Mukherjee** and A. S. Dhar, “New QL-QT Static Redundancy Method for Fault Tolerant Architecture Design,” International Conference on VLSI and Signal Processing (*ICVSP*), IIT Kharagpur, India, Jan. 2014, pp. 1-5.
24. **A. Mukherjee** and A. S. Dhar, “Design of a Self-Reconfigurable Adder for Fault-Tolerant VLSI Architecture,” IEEE International Symposium on Electronic System Design (*ISED*), IIEST Shibpur, Kolkata, India, Dec. 2012, pp. 92-96. DOI: 10.1109/ISED.2012.21.
25. **A. Mukherjee** and A. S. Dhar, “Design of a Fault-Tolerant Conditional Sum Adder,” 16th International Symposium on VLSI Design and Test *(VDAT)*, IIEST Shibpur, Kolkata, India, in Springer LNCS, Berlin, Heidelberg, vol. 7373, pp. 217-222, 2012. DOI: 10.1007/978-3-642-31494-0_25.

List of Sponsored Projects

1. *Development of complete resilient reconfigurable field programmable gate array (FPGA) with defect tolerant controller for payload designs in nano-satellites* (as Principal Investigator), sponsored by DST SERB, Duration: Jan 2024 to Jan 2027 (36 months), Budget: 30.57 lakhs.