

PROFORMA FOR BIO-DATA

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3. Institution: National Institute of Technology, Rourkela
4. Academic Qualification (Undergraduate Onwards)

Sl.No	Degree	Year	Subject/Discipline	University/Institution	% Marks or Grade
1.	Post Doc	2017	ECE (VLSI)	NUS Singapore	NA
2.	Ph.D	2015	E & ECE (VLSI)	IIT Kharagpur	NA
3.	MS	2009	E & ECE (VLSI)	IIT Kharagpur	8.97
4.	BE	2002	Instrumentation	Jadavpur University	76.4

5. Ph.D. Thesis details:

Title: Design of Performance Enhanced Current Steering DACs Based on Reused Distributed Binary Cells

Guide: Prof. Swapna Banerjee, Dept of E & ECE, VLSI Specialization

Institute: IIT Kharagpur

Year of award: 2015

6. Work experience (in chronological order):

Sl. No.	Designation	Name of the Institute/Organization	From Month-year	To Month-Year
1.	Asst Prof (Grade I)	NIT Rourkela	July 2014	Till-date
2.	Research Fellow	NUS Singapore	Jun 2016	Dec 2017
3.	Senior Project Officer	IIT Kharagpur	May2009	Dec 2013

7. Professional Recognition/ Award/ Prize/ Certificate/Fellowship received by the PI:

Sl.No.	Name of Award	Awarding Agency	Year
1.	National Scholarship for Secondary Examination	Government of India	1995
2.	Top-9 Designer in Cadence Design Contest	CADENCE DESIGN SYSTEMS	2008

3.	Students Team “ Digital Designers Rourkela” was selected in top 100 in Digital India RISC-V (DIR-V) Grand Challenge 2025” competition under C2S Chip to Start Up program.	MeitY Govt. of India	2025
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8. Publications (List of papers published in SCI Journals, in year wise descending order)

S.No.	Author(s)	Full title	Name of the Journal	Vol	Page	Year
1.	Smrutilekha Samanta and Santanu Sarkar	Mismatch error compensation of hybrid CS-DAC to achieve high figure of merit utilizing on-chip self-healing assisted swap-enabled randomization technique	International Journal of Circuit Theory and Applications, Wiley Publications DOI: https://doi.org/10.1002/cta.3875	52 (5)	2191 - 2204	Nov 2023
2.	Smrutilekha Samanta and Santanu Sarkar	A 10-bit CS-DAC using Fully Random Rotation based DEM and Code Independent Output Impedance Compensation	AEU International Journal of Electronics and Communications, Science Direct, Elsevier DOI: https://doi.org/10.1016/j.aeue.2023.154528	161	1545 - 28	March 2023
3.	Karim Ali Ahmed, Jinq Horng Teo, Santanu Sarkar , Massimo Alioto	Dual-Mode Conversion Gating, Comparator Merging and Reference-Less Calibration for 2.7X Energy Reduction in SAR ADCs under Low-Activity Inputs	IEEE Solid-State Circuits Letters DOI: 10.1109/LSSC.2023.3246063	6	57-60	Feb 2023
4.	Smrutilekha Samanta	A Pairwise Swap Enabled	IEEE Transactions on Very Large Scale	30 (9)	1332 -	Sept 2022

	and Santanu Sarkar	Randomized DEM Addressing Intersegment Mismatch for Current Steering Digital-to-Analog Converters	Integration Systems (TVLSI) DOI: 10.1109/TVLSI.2022.3183353		1340	
5.	Smrutilekha Samanta and Santanu Sarkar	An on-chip partial self-healing calibration technique for 10-bit reused distributed current steering DAC	Analog Integrated Circuits and Signal Processing, Springer Nature DOI: doi.org/10.1007/s10470-022-02096-x	113	353-360	Sept 2022
6.	Santanu Sarkar and Swapna Banerjee	A 10-bit High-Performance DAC in 180-nm CMOS with high-FOM	Analog Integrated Circuits and Signal Processing, Springer DOI: 10.1007/s10470-014-0309-x	80	59-68	July 2014
7.	Santanu Sarkar and Swapna Banerjee	An 8-bit Low Power DAC with Re-Used Distributed Binary Cells Architecture for Reconfigurable Transmitters	Microelectronics Journal, Elsevier DOI: 10.1016/j.mejo.2014.03.014	45	666-677	June 2014

9. Detail of Patents

Sl.No	Patent Title	Name of Applicant(s)	Patent No.	Award Date	Agency/Country	Status
1.	Distributed Binary Cells Realizing Hybrid Current Steering Architecture Based Digital to Analog Converter	Santanu Sarkar, Swapna Banerjee (IIT Kharagpur)	493605	03/01/2024	IIT Kharagpur, India	Granted

2.	Personalized Pollution Management (PPM) System	Santos K. Das, Santanu Sarkar and others. (NIT Rourkela)	527239	15/03/2024	NIT Rourkela, India	Granted
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10. Books/Reports/Chapters/General articles etc.

S.No	Title	Author's Name	Publisher	Year of Publication
1.	Comparative Study of the Design and Analysis of Ripple Carry Adder Using Reversible Logic Gates	Faeq Hussain and Santanu Sarkar	Recent Trends in Intelligent Systems and Next Generation Wireless Communication (Chapter 31), Proceedings of IIWCS 2024, ISBN 978-981-96-4740-8	2025
2.	Design and Development of Power-Efficient SAR ADC with Dual-Path Switching and Triple-Tail Comparator for Biomedical Signal Processing	Deepika Kumaradasan, Sougata K Kar and Santanu Sarkar	Recent Trends in Intelligent Systems and Next Generation Wireless Communication (Chapter 6), Proceedings of IIWCS 2024, ISBN 978-981-96-4740-8	2025
3.	Designing an 8-bit CMOS Low Glitch Digital-to-Analog Converter	Santanu Sarkar	LAP LAMBERT, ISBN CODE: 978-3-8383-9082-6,	2010

11. List of projects implemented

Project Title	Funding Agency	Duration	Sanction Cost	PIs / Co-PI name
Design and development of Mixed Signal Soc for Sensor Application in	ISRO, RESPOND	3 Years (March 2023-march 2026)	50.67 lakh	PI: Santanu Sarkar

SCL 180nm				
Development of a Closed-loop Integrated MEMS Capacitive Accelerometer for Inertial and Navigation Systems	SERB-CRG	5 Years (Feb 2020-Feb 2025)	58.96 lakh	Co-PI: Santanu Sarkar PI: Sougata K Kar
Intelligent Surveillance Data Retriever (ISDR) for Smart city Applications	Imprint-I, MHRD	5 Years (July 2017-July 2022)	386 lakh	Co-PI: Santanu Sarkar PI: Santosh K Das

12. List of Technology Developed/Demonstrated:

Sl.No.	Title	Year	Institution	Brief Detail	References
1.	Design of a 12-bit SAR ADC in 40 nm CMOS Multi-Vth Low Power TSMC Technology	2023	NUS, Singapore	Design and development of a 12-bit low power analog-to-digital converter.	Karim Ali Ahmed, Jinq Horng Teo, Santanu Sarkar, and Massimo Alioto, "Dual-Mode Conversion Gating, Comparator Merging and Reference-Less Calibration for 2.7X Energy Reduction in SAR ADCs under Low-Activity Inputs," IEEE Solid-State Circuits Letters, Feb 2023, doi: 10.1109/LSSC.2023.3246063.
2.	Design of 6-bit 100 MSPS Current Steering DAC in 180 nm	2022	NIT Rourkela	Design and development of 6-bit digital-to-analog converter	S. Samanta and S. Sarkar, "A Pairwise Swap Enabled Randomized DEM Addressing

	UMC CMOS Technology			for prototyping a novel Pairwise Swap Enabled Randomized DEM architecture	Intersegment Mismatch for Current Steering Digital-to-Analog Converters,” in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 30, no. 9, pp.1332-1340, Sept. 2022, doi: 10.1109/TVLSI.2022.3183353.
3.	Design of 8-bit 100 MSPS Current Steering DAC in 180 nm CMOS Technology	2009	IIT Kharagpur	Design and development of 8-bit digital-to-analog converter for a sponsored project of SAC, ISRO.	Santanu Sarkar and Swapna Banerjee, “An 8 bit Low Power DAC with Re-Used Distributed Binary Cells Architecture for Reconfigurable Transmitters”, Microelectronics Journal, Elsevier, vol. 45, issue 6, June 2014, pp. 666-677.
4.	Design of 10-Bit 500 MSPS Current Steering DAC in 180 nm CMOS Technology	2014	IIT Kharagpur	Design and development of 10-bit digital-to-analog converter for a sponsored project of SAC, ISRO.	Santanu Sarkar and Swapna Banerjee, “A 10- bit High-Performance DAC in 180-nm CMOS with high-FOM”, Analog Integrated Circuits and Signal Processing, Springer, vol. 80, issue 1, July 2014, pp. 59-68.

13. Conference Papers:

1. Mirza Amanullah Baig, Adyasha Mishra and Santanu Sarkar, “Low Power ALU Design using Pre-Computational LUT for RV32M Processor”, IEEE INDISCON 2025 conference, August 21–23, 2025, at NIT Rourkela, Odisha, India.
2. Deepika Kumaradasan, Sougata K Kar and Santanu Sarkar, “A Low-Power 10-bit SAR ADC with splitting decoder for Implantable Pacemakers”, IEEE INDISCON 2025 conference, August 21–23, 2025, at NIT Rourkela, Odisha, India.
3. Ipsita Dash, Sougata Kumar Kar, Santanu Sarkar, “Noise Analysis in Switched Capacitor-Based Differential Capacitive Interfacing Circuits”, 2024/12/19, 2024 IEEE 21st India Council International Conference (INDICON), pp. 1-4, doi: 10.1109/INDICON63790.2024.10958540.
4. Ipsita Dash, R Maheshwari, Sougata Kumar Kar, Santanu Sarkar, “A Capacitance Mismatch Cancellation Technique for Differential Capacitive Interfacing Circuit”, 2024/12/19, 2024

- IEEE 21st India Council International Conference (INDICON), pp. 1-5, doi: 10.1109/INDICON63790.2024.10958311.
5. M. A. Baig and S. Sarkar, "A 13-Bit Resolution High Performance Time Domain Comparator Using Intermediate Buffer Based VCO," TENCON 2024 - 2024 IEEE Region 10 Conference (TENCON), Singapore, Singapore, 1-4 Dec 2024, pp. 1545-1548, doi: 10.1109/TENCON61640.2024.10902767.
 6. D. Kumaradasan, S. K. Kar and S. Sarkar, "An 8-bit 1 MS/s Low-Power SAR ADC with an Enhanced EPC for Implantable Medical Devices," 2024 IEEE Computer Society Annual Symposium on VLSI (ISVLSI), Knoxville, TN, USA, July 1-3 2024, pp. 9-14, doi: 10.1109/ISVLSI61997.2024.00014.
 7. D. Kumaradasan, S. K. Kar and S. Sarkar, "A Low-Power 10-bit SAR ADC with an Integrated CDAC and C-MOSCAP DAC for Implantable Pacemakers," 2024 28th International Symposium on VLSI Design and Test (VDAT), Vellore, India, 1-3 September 2024, pp. 1-6, doi: 10.1109/VDAT63601.2024.10705705.
 8. Faeq Hussain and Santanu Sarkar, "Design and FPGA Implementation of Five Stage Pipelined RISC-V Processor", IEEE 2024 9th International Conference for Convergence in Technology (I2CT), Pune, Maharashtra, India, 5-7 April 2024, doi: 10.1109/I2CT61223.2024.10544184.
 9. Deepika Kumaradasan, Sougata K Kar and Santanu Sarkar, "Power-Efficient SAR ADC with Dual Path Switching and Triple Tail Comparator for Biomedical Signal Processing", National conference on Intelligent Systems, IoT, and Wireless Communication for the Society (IIWCS), 16-17 Feb 2024, NIT Rourkela, India.
 10. Faeq Hussain and Santanu Sarkar, "Comparative Study of the Design and Analysis of Ripple Carry Adder using Reversible Logic Gates", National conference on Intelligent Systems, IoT, and Wireless Communication for the Society (IIWCS), 16-17 Feb 2024, NIT Rourkela, India.
 11. Bhubaneswar Das, Santanu Sarkar and K. K. Mahapatra, "Design and Development of Real-Time Capacitive Sensor Readout Circuit for Small Gap Measurement", National conference on Intelligent Systems, IoT, and Wireless Communication for the Society (IIWCS), 16-17 Feb 2024, NIT Rourkela, India.
 12. Deepika Kumaradasan, Sougata K Kar and Santanu Sarkar, "An 8-bit 100 kS/s Low Power SAR ADC with Modified EPC for Bio-Medical Applications", IEEE Silchar Subsection Conference (SILCON), November 3-5, 2023, doi: 10.1109/SILCON59133.2023.10404914.
 13. S. Samanta and S. Sarkar, "Dynamic Switching Compensation Technique Mitigating Code-Dependent Switching Distortion in CS-DACs", 2022 IEEE 19th India Council International Conference (INDICON), 24-26 November, 2022, doi: 10.1109/INDICON56171.2022.10039778.
 14. Smrutilekha Samanta and Santanu Sarkar, "A 10-bit 500 MSPS Segmented CS-DAC of > 77 dB SFDR upto the Nyquist with Hexa-decal biasing", IEEE 24th International Symposium on VLSI Design and Test (VDAT), 23-25 Jul, 2020, IIT Bhubaneswar, Odisha. DOI:10.1109/VDAT50263.2020.9190402.
 15. Smrutilekha Samanta and Santanu Sarkar, "A 1.8 V 8-bit 500 MSPS Segmented Current Steering DAC with > 66 dB SFDR", IEEE Computer Society Annual Symposium on VLSI (ISVLSI20), Jul 6-8, 2020, Limassol, CYPRUS. DOI:10.1109/ISVLSI49217.2020.00013.
 16. Sachin Khandagale and Santanu Sarkar, "A 6-Bit 500 MSPS Segmented Current Steering DAC with On-Chip High Precision Current Reference," in IEEE International Conference on

Computing, Communication and Automation (ICCCA2016), 29-April 2016. DOI: 10.1109/CCAA.2016.7813858.

17. Sachin Khandagale and Santanu Sarkar, "An 8-Bit 500 MSPS Segmented Current Steering DAC Using Chinese Abacus Technique," in 20th International Symposium on VLSI Design and Test (VDATE), 24-May 2016. DOI: 10.1109/ISVDATE.2016.8064903.
18. Santanu Sarkar and Swapna Banerjee, "A 10-bit 500 MSPS Segmented DAC with Distributed Octal Biasing Scheme", International Conference on Signal Processing, Computing and Control (ISPCC 15), Solan, Himachal Pradesh, India, 25-Sept 2015, pp. 145-148, DOI: 10.1109/ISPCC.2015.7375014.
19. Santanu Sarkar and Swapna Banerjee, "A 10-bit 500 MSPS Segmented DAC with Optimized Current Sources to Avoid Mismatch Effect", IEEE Computer Society Annual Symposium on VLSI (ISVLSI15), Montpellier, France, 09-July 2015, pp. 172-177. DOI: 10.1109/ISVLSI.2015.87.
20. Santanu Sarkar and Swapna Banerjee, "500 MHz Differential Latched Current Comparator for Calibration of Current Steering DAC", IEEE Student's Technology Symposium (IEEE TechSym), IIT Kharagpur, 28-Feb 2014, pp. 309-312. DOI: 10.1109/TechSym.2014.6808066.
21. Santanu Sarkar and Swapna Banerjee, "An 8-bit 1.8V 500 MSPS CMOS Segmented Current Steering DAC", Proceedings of IEEE Computer Society Annual Symposium on VLSI 2009 (ISVLSI), Tampa, Florida, 14-May, 2009, pp. 268-273. DOI: 10.1109/ISVLSI.2009.12.
22. Santanu Sarkar, R. S. Prasad, S. K. Dey, V. Belde and S. Banerjee, "An 8-bit, 1.8V, 500MS/s CMOS DAC with a Novel Four Stage Current Steering Architecture", IEEE International Symposium on Circuits and Systems (ISCAS), Seattle, Washington, USA, 19-May 2008, pp. 149-152. DOI: 10.1109/ISCAS.2008.4541376.
23. Santanu Sarkar, S. K. Dey, V. Belde and S. Banerjee, "A Novel and Simple, Supply Voltage and Temperature Compensated Current Reference", Conference on Advances in Space Science and Technology (CASST), IIT Kharagpur, Jan 2008, pp. 1-3.

14. Workshops conducted:

1. High end Karyashala workshop on "Analog and Digital VLSI Design Flow and Embedded System Design" organized from July 4, 2022, to July 13, 2022 in physical mode by Santanu Sarkar and Sougata Kumar Kar in the ECE Dept. of NIT Rourkela, Sponsored by SERB, Govt. of India, under Karyashala, Accelerate Vigyan scheme.
2. Workshop conducted on "Micro-Sensors and Interfacing Circuits (MSIC-2022)" organized by Sougata Kumar, Santanu Sarkar and Sudip Kundu, from 18 July-22 July 2022 in the ECE Dept. of NIT Rourkela, Sponsored by SERB, Govt. of India.

15. Brief note:

Presently, Dr. Sarkar is working as an Asst. Prof. in the ECE department of NIT Rourkela. Presently, Dr. Santanu Sarkar is working as a principal investigator for the development of a mixed signal sensor interface IC for Aerospace applications for ISRO. Dr. Sarkar, also worked as Co-PI in two other SERB sponsored projects. Dr. Santanu has organized two workshops in

the domain of VLSI Design and MEMS based system design along with other co-coordinators. Dr. Sarkar has published 7 internationally acclaimed SCI index high quality journals and more than 20 international and national conference papers. Dr. Sarkar has experience of tape out of Integrated Circuits in 180 nm and 40 nm CMOS technologies. Dr Sarkar has expertise in design of mixed signal circuits and data converters. Dr Sarkar has successfully taped out three current steering DAC ICs in 180 nm CMOS technology. Dr. Sarkar, completed his post-doctoral fellowship from the ECE department of National University of Singapore (NUS). As a part of his post-doctoral research, he has taped out a 12-bit Successive Approximation Register (SAR) based ADC in 40 nm CMOS technology.

16. Referees

Name	Designation	Organization	Email id
Dr. Swapna Banerjee	Retired Prof.	IIT Kharagpur	swapna.bnj@gmail.com
Dr. Massimo Alioto	Prof, NUS	NUS	massimo.alioto@gmail.com