Instruction Enhancement Program
On
Design Verification and Hardware Security
NIT Rourkela

(1st July 2019 to 5th July 2019)

Objectives: -

- This Instruction Enhancement Program (IEP) provides: -
  - A hands-on introduction to the Digital design verification and System Verilog language to verify a device under test with object-oriented methodologies targeting coverage-driven constrained-random test environments.
  - System Verilog Assertion language and its use in creating reusable, scalable assertions and assess the effectiveness of your verification programme.
  - Formal verification and to learn how to write effective assertions to find and fix bugs
  - Introduction to a Hardware Security and its different dimensions.

Syllabus: -

- System Verilog Design Verification-I: - The concept of Device under test (DUT), Complexity of verification, lexical elements of system Verilog (SV), Layered testbench and SV verification environment.
- System Verilog Design Verification-II: - Basics of SV testbench, concurrency in system Verilog, object oriented programming, encapsulation and randomization.
- System Verilog Design Verification –III: - Inter-thread communications, mailbox, code coverage, functional coverage and building efficient SV testbenches. System Verilog UVM.
- Formal Verification (FV): -Importance of FV, Challenges in implementing FV, Boolean Algebra, Boolean satisfiability, Basic assertion concepts, immediate assertions, concurrent assertions, Sequences, clocks, resets and coverage.
- Hardware Security: - Reasons for raise of hardware security issues, IC Counterfeiting, IP piracy, Hardware Trojans, Debug security and applications of Physical Unclonable Functions (PUF).

References: -

1. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features by Chris Spear , Greg Tumbush, Springer; 3rd ed. 2012 edition.
2. SystemVerilog Assertions and Functional Coverage: Guide to Language, Methodology and Applications, by Ashok B. Mehta, Springer; 2014 edition.
3. Formal Verification: An Essential Toolkit for Modern VLSI Design 1st Edition by Erik Seligman , Tom Schubert , M V Achutha Kiran Kumar, Morgan Kaufmann; 2015.
4. Clifford E. Cummings, “SystemVerilog Assertions - Bind files & Best Known Practices for Simple SVA Usage”
5. Wolfgang Ecker, VolkanEsen, Thomas Kruse, Thomas Steininger, Peter Jensen “SystemVerilog Assertions - Techniques, Tips, Tricks, and Traps”
6. Don Mills, Stuart Sutherland “SystemVerilog Assertions Are For Design Engineers Too!”
7. Getting Started with UVM: A Beginner's Guide 1st Edition, by Vanessa R. Cooper, Verilab Publishing, 2013

8. Introduction to Hardware Security and Trust Editors: Tehranipoor, Mohammad, Wang, Cliff (Eds.), Springer-Verlag New York, 2012.

Date and Schedule: - (1st July 2019 to 5th July 2019)

Sl. No	Date and Day	Classroom Sessions			Lab Session
		9 AM to 10 AM	10AM to 11AM	11.15 AM to 12.30 PM	1.30 PM to 4.30PM
1	Monday (01-07-19)	Inauguration	Advanced Digital Design	Introduction to Verification and System Verilog	Code Coverage and Functional Coverage
2	Tuesday (02-07-19)	System Verilog (SV) Testbench, lexical elements of SV	Encapsulation and Randomization	Mailbox, inter thread communications	System Verilog Testbench (3 to 4 examples)
3	Wednesday (03-07-19)	System Verilog Testbench	Universal Verification Methodology -I	Universal Verification Methodology-II	System Verilog Testbench and UVM Testbench
4	Thursday (04-07-19)	Introduction to Formal Verification	SV assertions-I	SV assertions -II	Experiments on formal verification
5	Friday (05-07-19)	Formal Verification	Introduction and advancements in Hardware Security		Simulation of Hardware Trojan and Valedictory Ceremony

Number of Participants: -

- We can accommodate 25 participants. (Cadence 10 licenses and Synopsys 5 licences),

Any Software/Hardware requirement from participant's side: -

- No .We will be hosting with our lab infrastructures (PCs and Tools given by SMDPC2SD).

Boarding and Lodging details: -NIT Guest House is available on these dates. We can accommodate the participants there. The budget details for boarding and lodging is included in the budget below.

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