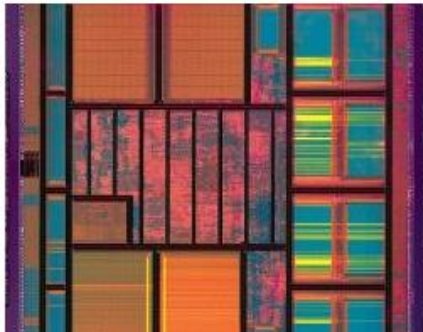


A Short-Term Course on  
**VLSI DESIGN USING  
CAD TOOLS  
VLSI-CAD 2026  
(Offline)**

**(18<sup>th</sup> May – 30<sup>th</sup> May 2026)**



**Coordinators**

A.K.Swain

**Co-coordinators**

K.K.Mahapatra

D.P.Acharya



Dept. of Electronics & Comm. Engg.  
National Institute of Technology  
Rourkela – 769008.

**COURSE OBJECTIVE:**

Very Large Scale Integrated Circuits (VLSI) continue to be the prime medium for realizing modern Electronic Systems. With the semiconductor industry's relentless pursuit of higher performance and lower power, there is a persistent demand for professionals skilled in the latest design methodologies and tools.

The primary objective of this course is to train students and professionals in advanced VLSI design fundamentals and provide them with intensive, **hands-on experience with the same industry-standard Computer-Aided Design (CAD) tools** used by leading semiconductor companies.

**Selected candidates will be offered an internship opportunity for 30–60 days based on their course performance, with no extra fees.**

**COURSE CONTENTS:**

The program is divided into two comprehensive modules, allowing participants to focus on specific areas of the VLSI design flow.

**Module-I RTL Design, Simulation, and FPGA Prototyping**

**(18<sup>th</sup> May – 23<sup>rd</sup> May 2026)**

- ❖ Digital Logic Design
- ❖ RTL Design using HDL (Verilog)
- ❖ Functional Simulation & Testbench Writing
- ❖ Logic Synthesis & Optimization
- ❖ FPGA Architecture & Design Flow
- ❖ FPGA Prototyping: Implementation, Place & Route
- ❖ Timing Closure for FPGAs
- ❖ On-board Testing and Debugging

**Module-II RTL-to-GDSII ASIC Design Flow**

**(25<sup>th</sup> May – 30<sup>th</sup> May 2026)**

- ❖ ASIC Design Methodology Overview
- ❖ RTL to GDSII Flow Introduction
- ❖ Logic Synthesis for ASICs
- ❖ Design for Testability (DFT)
- ❖ Floor-planning and Power Planning
- ❖ Placement and Routing
- ❖ Clock Tree Synthesis (CTS)
- ❖ Static Timing Analysis (STA)
- ❖ Physical Verification (DRC & LVS)

**VLSI CAD Tools To Be Used:**

Synopsys, Cadence, AMD Xilinx Vivado.

**Prerequisite:** Knowledge of Basic and Digital Electronics is mandatory.

**INTENDED AUDIENCE:**

This program is open to B. Tech students from the 4<sup>th</sup> semester onwards, M. Tech and Ph.D. scholars, faculty members, and professionals from industry and R&D organizations in Electronics, Electrical, and Computer Science Engineering. It is designed for participants who wish to gain practical expertise in VLSI design using industry-standard CAD tools. Selected participants may also get the opportunity to continue with a 45–60-day internship in the area of VLSI design based on their performance.

**ABOUT NIT ROURKELA:**

**National Institute of Technology (NIT), Rourkela**, established in 1961 as Regional Engineering College, is one of India's premier institutes for engineering education, research, and innovation. The institute has consistently been ranked among the top engineering institutions in India by the **National Institutional Ranking**

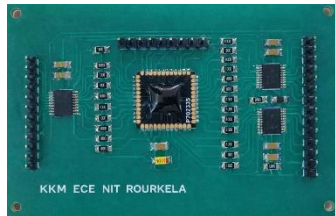
Framework (NIRF), Government of India, and achieved Rank 13 in NIRF Ranking 2025.



Website: [www.nitrkl.ac.in](http://www.nitrkl.ac.in)

### ABOUT THE VLSI Group

The VLSI and Embedded Systems Group at NIT Rourkela, established in 2005 within the Department of Electronics and Communication Engineering (ECE), focuses on VLSI design, CAD tools, Embedded systems, and hardware security. Since 2006, the group has trained many undergraduate, postgraduate, and research scholars in chip design and semiconductor technologies supported by SMDP. Currently supported by the C2S (Chip to Startup) program of MeitY, Government of India, the lab has successfully designed and fabricated four IC chips and presented its IC design work at SEMICON India 2025 (C2S0017).



### REGISTRATION AND FEES:

Module	Student	Faculty	Industry/ R&D
*Module-I	5000/-	6000/-	8500/-
*Module-II	5000/-	6000/-	8500/-
Both	8000/-	11,000/-	16000/-

\* Fees include GST

### MODE OF PAYMENT:

Transfer the Fee amount using UPI or NEFT. Please mention in remarks: "STC on VLSI-CAD 2026"

### ACCOMMODATION:

UPI ID:	01389517841@sbi
Account Number	10138951784
Account Name	CONTINUING EDUCATION NIT ROURKELA
Bank	State Bank of India
Branch	NIT Rourkela Campus
IFSC	SBIN0002109

Accommodation is available in the NIT Rourkela Hostels on a sharing basis, subject to availability. The charges per day of 250/- (Food Included) are exclusive of GST and cover only the bed space. Students must arrange their own bedding materials.

### Important Notes:

- Accommodation is provided on a first-come, first-serve basis due to limited seats (50 participants only).
- Charges cover only the bed space; students must bring their own bedding (pillow, mattress, bedsheet, etc.).

### IMPORTANT DATES:

Last Date of Registration: 30/04/2026  
Selection Letters to Be Mailed: 05/05/2026  
Course Commences On: 18/05/2026

### CONTACTS:

A. K. Swain : 94373 41298(M)  
K. K. Mahapatra: 0661-2462454(O)  
D. P. Acharya : 0661-2462463(O)  
VLSI Lab : 0661-2464458

### MAILING ADDRESS:

Coordinator, VLSI Design & Related CAD Tools  
Dept. of ECE  
National Institute of Technology  
Rourkela-769008, Odisha, INDIA.  
Phone:0661-2464458  
Email : vlsi.nitrkl@gmail.com

### IMPORTANT NOTE

**Seat Availability:** Only 50 seats are available for this program.

**Registration Mode:** Admissions will be granted on a First-Come, First-Serve basis. Early registration is strongly recommended to avoid disappointment.

**Confirmation:** Your participation will be confirmed only upon successful completion of registration and payment of the required fees, along with submitting your details in the Google Form.

**Deadline:** 30th April 2026, or until seats are filled, whichever is earlier.



Register to Secure Your Spot