National Institute of Technology Rourkela

Defence Seminar

Seminar Title	: Post-Manufacturing Sensing and Healing Techniques in Analog and Radio Frequency Integrated Circuits
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Venue	: EC 303, EC Seminar Hall
Date and Time	: 21 May 2025 (3:30pm)

Abstract : Analog and radio frequency integrated circuits (RFICs) are increasingly susceptible to process variations, leading to significant performance degradation and low fabrication yields. The conventional strategy of over-designing circuits to address this issue imposes significant area and power overheads, making it unsuitable for high-speed and portable applications. An alternative approach is to sense and heal the chip performance impairment using suitable tuning control in post-manufacturing stage for yield improvement. Test time reduction in post manufacturing performance sensing and healing of analog and RF circuits is a challenging task, that requires development of advanced sensing techniques integrated with efficient healing algorithm. This work focuses on the different post-manufacturing sensing and healing techniques for analog circuits with an objective of reduction in test time and test cost.

A Machine Learning (ML) based indirect sensing and one-step healing framework have been used in this work. Non-intrusive process variation sensors (PVSs) are used for performance sensing. Appropriate Test Signatures (TSs) are extracted from the designed PVSs through identification of vital process parameters affecting the performance. A current starved voltage controlled oscillator (CSVCO), which is an integral part of a phase locked loop (PLL) is considered as the test circuit to validate the proposed sensing and healing framework.

The performance sensing and healing require a large volume of data for better model training. In order to reduce the lengthy simulation time in extracting the data for effective model training, a Generative Adversarial Network (GAN) is used to generate synthetic data during the design phase. The proposed approach expedites the design process, and reduces the design costs for building effective ML model for performance prediction.

Finally, an on-chip approach for autonomous sensing and healing of long term jitter in PLL is proposed. A compact and energy efficient Built -in &ndash Jitter Sensor (BIJS) is proposed to sense the Long-Term Jitter (t_{LTJ}) in a PLL. Also, a digital self-healing circuit is proposed to heal the (t_{LTJ}) of a process-impaired PLL to acceptable limit.