

**Department of Electronics & Communication Engineering  
N I T Rourkela**

**Course Title : CMOS Digital IC Design**

May 7, 2007

**Course Schedule**

Day	Lectures	Title	Laboratory
May 7 (Mon)	L1 L2 L3 L4	Registration & Inauguration VLSI Design Introduction Fabrication Process - 1 Introduction to SPICE & Tanner tools (L-EDIT) -1	Lab 1: Layout of Basic Circuit Elements
May 8 (Tue)	L5 L6-L7 L8	Fabrication Process - 2 Introduction to MOSFET Introduction to SPICE & Tanner tools - 2	Lab 2: Layout & Extraction of CMOS Inverter
May 9 (Wed)	L9-L10 L11 L12	CMOS transistor Characteristics Fabrication Process - 3 Stick diagram - 1	Lab 3: Calculation of Power, Delay, Noise Margin of a CMOS Inverter
May10 (Thu)	L13 L14-L15 L16	Stick diagram - 2 CMOS Inverter Characteristics Basic digital circuits & Logic style	Lab 4: Layout and Simulation of Basic Gates - 1
May11 (Fri)	L17-L18 L19-L20	Combinational circuits Scaling	Lab 5: Layout and Simulation of Basic Gates - 2
May12 (Sat)	L21-L22 L23-L24	Sequential Logic Circuit VLSI Application to DSP	Lab 6: Layout and Simulation of Basic Gates - 3
May14 (Mon)	L25 L26  L27-L28	Introduction to High level Design VLSI Design: an overview & EDA tools VHDL modeling styles	Lab 7: Simulation of Basic Gates - 1
May15 (Tue)	L29-L30  L31-L32	VHDL -1  Combinational & Sequential circuit design in VHDL	Lab 8: Simulation of Basic Gates - 2
May16 (Wed)	L33-L34 L35-L36	VHDL -2 Logic Synthesis	Lab 9: Simulation of Basic Gates - 3

May17 (Thu)	L37-L38 L39-L40	Different Adder Architecture FPGA Architecture	Lab 10: Simulation of Basic Gates - 4
May18 (Fri)	L41-L42 L43-L44	SPECIAL TOOL DEMO ( <b>SYNOPTIS, MENTOR GRAPHICS</b> )	Lab 11: Downloading to FPGA

**Tools for Back-end: T-SPICE**

**Tools for Front-end: XILINX**

**Each Lecture will be of 55 Minutes duration and Laboratory will be of 3 Hour duration.**

Recommended Reference:

1. Rabaey, J. M., Chandrakasan A, Nikolic B, "Digital Integrated Circuits, A Design Perspective", Second Edition, Prentice Hall
2. Perry D. L,  
VHDL Programming By Examples, TMH