SUMANTA PYNE

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EDUCATION

Indian Institute of Technology Kharagpur
Doctor of Philosophy *(Ph.D.)* ***in Computer Science & Engineering*** ***February 2016***
Dissertation title - ***Power Aware Software***
Supervisor - Prof. Ajit Pal

Bengal Engineering and Science University, Shibpur
(presently Indian Institute of Engineering Science and Technology, Shibpur)
Master of Engineering *(M.E.)* ***in Computer Science & Engineering*** ***June 2009***
Thesis title - ***Pinball Routing Elimination with Route Optimization in Multihomed Mobile Networks***
Supervisor - Prof. Sulata Mitra

Meghnad Saha Institute of Technology
Bachelor of Technology *(B.Tech)* ***in Computer Science & Engineering*** ***June 2005***
from West Bengal University of Technology
(presently Maulana Abul Kalam Azad University of Technology)
Project title - ***Online Hotel Reservation System***
Supervisors - Prof. Baishali Ghosal and Mr. Farooq Ahmed

EXPERIENCE

National Institute of Technology, Rourkela **July 2015 - Present**
Assistant Professor, Dept. of Computer Science & Engineering

Courses taken – Data Structures and Algorithms, Programming Laboratory, Microprocessor and micro-controllers (Theory & Laboratory), Hardware Description Language Laboratory, Computer System Architecture, Data Communication (Theory & Laboratory), Compiler Design (Theory & Laboratory), Design and Analysis of Algorithms (Theory & Laboratory), Discrete Mathematics, Product Development Laboratory, Seminar and Technical Writing, Real-Time Systems Design, Formal Languages and Automata Theory, Short Term Industrial/Research Experience.

Indian Institute of Technology Kharagpur **January 2010 - May 2015**
Research Scholar, Dept. of Computer Science & Engineering

- **Worked on software techniques for reduction of dynamic and leakage power dissipation in processors based on CMOS technology.**
  - **Power aware software prefetching using DVFS and prefetch distance scaling.**
  - **Branch target buffer energy reduction by translation of multi-way branches.**
  - **Loop unrolling with Gray code sequence of accessing array elements.**
  - **Loop unrolling with power gating of functional units.**
  - **Energy efficient scheduling of OpenMP loops using DVFS and DVTS.**
- **Teaching Assistantship – Programming and Data Structures (Theory & Laboratory), Low Power Circuits and Systems, Advanced Computer Architecture.**

Bengal Engineering and Science University, Shibpur **July 2009 - December 2009**
Researcher, Dept. of Computer Science & Technology

- **Integration of Mobile Adhoc Network (MANET) with Mobile Network to form (MANEMO).**
- **Designed MANEMO for Fishing Trolleys in Deep Sea.**

Bengal Engineering and Science University, Shibpur **July 2007 - June 2009**
Post graduate Scholar, Dept. of Computer Science & Technology

- **Worked on multihomed and nested mobile networks.**
  - **Fuzzy logic based route optimization multihomed mobile networks.**
  - **Elimination of pinball routing in nested mobile networks.**
  - **Design of NEMO_SIM simulator.**
- **Teaching Assistantship – Programming Laboratory.**

Techno India College of Technology, Kolkata
(presently Techno International, New Town) **January 2006 - June 2007**
Lecturer, Dept. of Computer Science & Engineering

Courses taken – Introduction to Programming (Theory & Laboratory), Computer Organization, Data Structure Laboratory, Advanced Computer Architecture, Computer Architecture Laboratory.

Hi-Q Solutions, Kolkata **July 2005 - December 2005**
Programmer

Worked on Web technology, Micro-controller and Embedded System based applications.

RESEARCH INTERESTS

Low Power VLSI	**Software and hardware techniques for energy-efficient design**
Computer Architecture	**non-von Neumann architectures, in-memory computing**
Compiler Design	**Code generation for low power and in-memory computing**
Embedded Systems	**Battery-aware design**
Digital Microfluidics	**Scheduling, routing, placement, sample preparation**
Computer Networks	**Mobile networks, vehicular adhoc networks**

HONOURS/ACHIEVEMENTS/AWARDS

1. **Reviewer, 2023 Design Automation and Test Conference in Europe (DATE'23), 2022.**
2. **Faculty Advisor Appreciation Award, Inst. Counselling Serv., NIT Rourkela, 2022.**
3. **Mathematical Research Impact Centric Support (MATRICS) from Science and Engineering Research Board (SERB), Govt. of India for project titled "Modelling Hybrid Battery-Supercapacitors for Successive and Simultaneous Workloads in Embedded Systems", 2022.**
4. **Reviewer, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021.**
5. **Travel Grants from NIT Rourkela for oral presentation at**
   - **36^{th} Int'l. Conf. on VLSI Design & 22^{nd} Int'l Conf. on Embedded Systems (VLSID '23), Jan 8-12 2023, Hyderabad, India.**

- **32^{nd} Int'l. Conf. on VLSI Design & 18^{th} Int'l Conf. on Embedded Systems (VLSID '19), Jan 5-9 2019, NCR, New Delhi, India.**
- **ACM/IEEE Int'l. Symp. of Low Power Electronics & Design (ISLPED '18), July 23-25 2018, Seattle, WA, USA.**
- **28^{th} ACM Great Lakes Symp. on VLSI (GLSVLSI '18), May 23-25 2018, Chicago, IL, USA.**
- **31^{st} Int'l. Conf. on VLSI Design & 17^{th} Int'l. Conf. on Embedded Systems (VLSID '18), Jan 6-10, 2018 Pune, India.**

6. **Manuscript titled "MANEMO for Fishing Trolleys in Deep Sea" included in International Information System for the Agricultural science and technology (AGRIS), a database maintained by Food and Agriculture Organization, United Nations.**
7. **Doctoral Scholarship from Ministry of Human Resource Development (MHRD), Govt. of India, 2010.**
8. **GATE scholarship from MHRD, Govt. of India for M.E., 2007.**

PUBLICATION IN JOURNALS

14. **K. Kishori, *S. Pyne*, "In-memory Set Operations on Memristor Crossbar," accepted to appear in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, June 2023.**
13. **J. Swain, *S. Pyne*, "A bidirectional droplet routing in digital microfluidics biochip," *Microprocessors and Microsystems*, 98, April 2023.**
12. **J. Swain, *S. Pyne*, "A flooding based droplet routing protocol for digital microfluidic biochip Journal of Circuits, Systems, and Computers," *Journal of Circuits, Systems and Computers*, April 2023.**
11. **R. Kolluri, *S. Pyne*, "Quasi-Static Scheduling based Error Recovery for Digital Microfluidic Biochips," *Microprocessors and Microsystems*, 94, Sep 2022.**
10. **J. Swain, *S. Pyne*, "An MMSPEED based droplet Routing protocol for Digital Microfluidic Biochip," accepted to appear in *Informatica*, July 2022.**
9. **R. Kolluri, *S. Pyne*, "Droplet Routing based on Double Deep Q-Network Algorithm for Digital Microfluidic Biochips," *Journal of Circuits, Systems and Computers*, July 2022.**
8. **R. Kolluri, *S. Pyne*, "A Hybrid Artificial Bee Colony Algorithm for Scheduling of Digital Microfluidic Biochip Operations," *Concurrency and Computation*, 33(13), July 2021.**
7. **R. Kolluri, *S. Pyne*, "Invasive Weed Optimization based Scheduling for Digital Microfluidic Biochip Operations," *Integration*, 76: 122-134, Jan 2021.**
6. ***S. Pyne*, "Scheduling of Dual Supercapacitor for Longer Battery Lifetime in Safety-Critical Embedded Systems with Power Gating," *IET Computers & Digital Tech.*, 13(6): 429-442, Nov 2019.**
5. ***S. Pyne*, A. Pal, "Energy Efficient Array Computations using Loop Unrolling with Partial Gray Code Sequence," *Journal of Low Power Electronics*, 11(2): 149-172, June 2015.**
4. ***S. Pyne*, A. Pal, "Runtime Leakage Power Reduction using Loop Unrolling and Fine Grained Power Gating," *Journal of Low Power Electronics*, 11(1): 16-36, Mar 2015.**

3. ***S. Pyne***, A. Pal, "Branch Target Buffer Energy Reduction Through Efficient Multiway Branch Translation Techniques," *Journal of Low Power Electronics*, 8(5): 604-623, Dec 2012.

2. S. Mitra, ***S. Pyne***, "Pinball Routing Elimination Algorithm for Multihomed Mobile Networks," *International Journal of Sensors, Wireless Communication and Control*, 1(2): 147-155, Dec 2011.

1. S. Mitra, ***S. Pyne***, "Fuzzy logic based route optimization in multihomed mobile networks," *Wireless Networks*, 17(1): 213-229, Jan 2011.

PUBLICATION IN CONFERENCE PROCEEDINGS

15. ***S. Pyne***, "Translation of Array Expressions for In-Memory Computation on Memristive Crossbar," *36th Int'l. Conf. VLSI Design & 22nd Int'l. Conf. Embedded Syst.* (VLSID '23), Jan 08-12 2023, Hyderabad, Telangana, India, 169-174.

14. ***S. Pyne***, "An Architectural support for Digital Microfluidic based Hot-Spot free Computing," *35th Int'l. Conf. VLSI Design & 21st Int'l. Conf. Embedded Syst.* (VLSID '22), Feb 26-Mar 02 2022, 156-161. (virtual event)

13. R. Kolluri, T. Rohith, ***S. Pyne***, "A heuristic algorithm for module placement in digital microfluidic biochips," *2nd Int'l. Conf. Advances VLSI & Embedded Syst.* (AVES '21), Dec 18-19 2021, Springer. (virtual event)

12. ***S. Pyne***, "Instruction Controlled In-memory Sorting on Memristor Crossbars," *34th Int'l. Conf. VLSI Design & 20th Int'l. Conf. Embedded Syst.* (VLSID'21), Feb 20-24 2021, Guwahati, Assam, India, 82-87, IEEE. (virtual event)

11. R. Kolluri, A. Tirkey, A. Sarkar, ***S. Pyne***, "Reinforcement Learning based Droplet Routing Algorithm for Digital Microfluidic Biochips," *24th Int'l. Symp. VLSI Design & Test* (VDAT '20), July 23-25 2020, Bhubaneswar, Odisha, India, 56:1-56:6, IEEE. (virtual event)

10. J. Swain, R. Kolluri, ***S. Pyne***, "A Proactive Wash droplet routing for Digital Microfluidics Biochip," *24th Int'l. Symp. VLSI Design & Test* (VDAT'20), July 23-25 2020, Bhubaneswar, Odisha, India, 51:1-51:4, IEEE. (virtual event)

9. V. Jaluka, R. Kolluri, ***S. Pyne***, "Virtual Droplet Routing Algorithm for Digital Microfluidic Biochips," *24th Int'l. Symp. VLSI Design & Test* (VDAT'20), July 23-25 2020, Bhubaneswar, Odisha, India, 44:1-44:6, IEEE. (virtual event)

8. R. Kolluri, J. V. Phani Kumar, J. Swain, ***S. Pyne***, "ABC-GNX: A Hybrid Algorithm for Scheduling of Digital Microfluidic Biochip Operations," *9th Int'l. Symp. Embedded Comput. & Syst. Des.* (ISED'19), Dec 13-14 2019, Kollam, Kerala, India, 1-5, IEEE.

7. J. Swain, R. Kolluri, ***S. Pyne***, "A Space Efficient Greedy Droplet Routing for Digital Microfluidic Biochips," *23rd Int. Symp. VLSI Design & Test* (VDAT'19), July 4-6 2019, Indore, Madhya Pradesh, India, 102-114, Springer.

6. R. Kolluri, J. V. Phani Kumar, ***S. Pyne***, "Heterogeneous Earliest Finish Time based Scheduling for Digital Microfluidic Biochips," *12th Int'l. Conf. Biomed. Electron. & Devices* (BIODEVICES'19), Feb 22-24 2019, Prague, Czech Republic, 175-182, SciTePress.

5. ***S. Pyne***, "Scheduling of Dual Supercapacitor for Longer Battery Lifetime in Systems with Power Gating," *32nd Int'l. Conf. VLSI Design & 18th Int'l. Conf. Embedded Syst.* (VLSID'19), Jan 5-9 2019, NCR, Delhi, India, 151-156, IEEE.

4. ***S. Pyne***, **"Scheduling of Hybrid Battery-Supercapacitor Control Instructions for Longevity in Systems with Power Gating,"** ***2018 ACM/IEEE Int'l. Symp. Low Power Electron. Des.*** **(ISLPED'18), July 23-25 2018, Seattle, WA, USA, 45:1-45:6, ACM.**

3. **J. Swain, *S. Pyne*, "Deadlock detection in Digital Microfluidics Biochip droplet routing,"** ***22nd Int'l. Symp. VLSI Design & Test*** **(VDAT'18), June 28-30 2018, Madurai, India, 242-253, Springer.**

2. ***S. Pyne***, **"An Architectural Support for Reduction of In-rush Current in Systems with Instruction Controlled Power Gating,"** ***28th ACM Great Lakes Symp. VLSI*** **(GLSVLSI'18), May 23-25 2018, Chicago, IL, USA, 487-490.**

1. ***S. Pyne***, **"Rescheduling of Power Gating instructions for reduction of In-rush current,"** ***31st Int'l. Conf. VLSI Design & 17th Int'l. Conf. Embedded Syst.*** **(VLSID'18), Jan 6-10 2018, Pune, Maharashtra, India, 25-30.**

MEMBERSHIP IN PROFESSIONAL SOCIETIES

- **Member of VLSI Society of India, Institution of Engineers (India), IET (UK), ACM and IEEE.**