Santanu Sarkar

NIT Rourkela, Odisha, India.

E-mail: sarkars@nitrkl.ac.in **Ph:** 0661-2462472

Objective: To be engaged in high class research in the field of analog integrated circuit design, where I can contribute, as well as can explore into new directions to enrich my knowledge. To supervise students in the field of Mixed Signal IC design. To publish high quality research work in reputed Journals.

Current Status: Assistant Professor (Grade-I) at the ECE Dept. of NIT Rourkela, Odisha, India, 769008.

Highlights of Educational Career

I. **Secondary** (Class X) – From the West Bengal Board of Secondary Education, India, 1995, **Percentage of Marks: 87.22 / 100 (Winner** of **Government Scholarship** ranked within **Top 5** position in **District** and within **Top 50** position **in State).**

II. **Higher Secondary** (Class XII) – From the West Bengal Council of Higher Secondary Education, India, 1997, **Percentage of Marks: 81.90 / 100 (**within **Top 10** position in **District).**

III. **Bachelor of Engineering** - From the Dept. of Instrumentation Engineering, **Jadavpur University**, West Bengal, India, 2002, **Percentage of Marks: 76.40 / 100.**

IV. **Master of Science** - From the Dept. of Electronics and Electrical Communication Engineering, IIT Kharagpur, West Bengal, India, 2009, **CGPA: 8.97 / 10.**

V. **PhD** –Dept. of Electronics and Electrical Communication Engineering, Indian Institute of Technology (IIT) Kharagpur, India, October 2015.
Thesis Title: Design of Performance Enhanced Current Steering DACs Based on Reused Distributed Binary Cells.

VI. **Post-doctoral Research** –Dept. of Electrical and Computer Engineering, National University of Singapore, Green-IC Lab, July 2016-Dec 2017.
Research Topic: Low power front-end analog circuit design and SAR ADC circuit design for HVAC Control MEMS interface.

Research Experience:

- Analog integrated circuit design, Digital-to-analog data converter IC design, Dynamic element matching circuit design for performance enhancement of the DAC, fabrication and testing of the designed DACs.
- Design and fabrication of Low Power SAR ADCs.
- Design and implementation of radiation hardened digital gates and LVDS driver in commercially available 0.18 μm CMOS process technology.
- Two successful tape out in 0.18 μm UMC CMOS process, one successful tape out in 40 nm TSMC technology and three successful tape out in 0.18 μm National Semiconductor CMOS process technology.
- Experience of IC testing.

Professional Experience

I. **Project Experience:** Worked in various research project sponsored by ISRO and DIT, Govt. of India.

Sl.No.	Title	Sponsor	Amount	From Date (Month-Year)	To Date (Month-Year)	Major Outcome
1.	Design and development of Mixed Signal Soc for Sensor Application in SCL 180nm	ISRO, RESPOND	50.67 Lakhs	March 2023	March 2026	To design Mixed Signal Sensor Interface Circuit **Role: PI**
2.	Intelligent Surveillance Data Retriever (ISDR) for Smart city Applications	Imprint-I, MHRD, Govt. of India	3.86 Crores	July 2017	July 2020	Product prototype, paper, patents **Role: Co-PI:**
3.	Development of a Closed-loop Integrated MEMS Capacitive Accelerometer for Inertial and Navigation Systems	SERB-CRG	58.96 Lakhs	Feb 2020	Feb 2023	To develop ASIC for Accelerometer with MEMS **Role: Co-PI:**

II. Work Experience:

Sl. No.	Designation	Name of the Institute/Organization	From Month-year	To Month-Year	Responsibility
1.	Asst. Prof	NIT Rourkela	July 2014	Till-date	Faculty ECE Dept. (VLSI)
2.	Research Fellow	NUS Singapore	Jun 2016	Dec 2017	Design and implementation of low power ADC
3.	Senior Project Officer	IIT Kharagpur, SRIC	May2009	Dec 2013	Design of Rad-hard Circuits
4.	Junior Project Officer	IIT Kharagpur, SRIC/ SMDP	Jan 2006	May 2009	Design of DAC
5.	Lecturer	Heritage Institute of Technology, Kolkata	April 2003	Jan 2006	Faculty Instrumentation Dept.

Publications

I. Publication in any of SCI or Scopus indexed Journal

1. Smrutilekha Samanta, **Santanu Sarkar**, "Mismatch error compensation of hybrid CS-DAC to achieve high figure of merit utilizing on-chip self-healing assisted swap-enabled randomization technique" **International Journal of Circuit Theory and Applications, Wiley Publications**, 30 November 2023; 1-14, https://doi.org/10.1002/cta.3875.

2. Karim Ali Ahmed, Jinq Horng Teo , **Santanu Sarkar** , Massimo Alioto, "Dual-Mode Conversion Gating, Comparator Merging and Reference-Less Calibration for 2.7X Energy Reduction in SAR ADCs under Low-Activity Inputs," **IEEE Solid-State Circuits** Letters, Feb 2023, doi: 10.1109/LSSC.2023.3246063.

3. S. Samanta and **S. Sarkar**, "A Pairwise Swap Enabled Randomized DEM Addressing Intersegment Mismatch for Current Steering Digital-to-Analog Converters," in **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, vol. 30, no. 9, pp.1332-1340, Sept. 2022, doi: 10.1109/TVLSI.2022.3183353.

4. S. Samanta and **S. Sarkar**, "An on-chip partial self-healing calibration technique for 10-bit reused distributed current steering dac," Analog Integrated Circuits and Signal Processing, Springer Nature, pp. 1–8, 2022, doi: https://doi.org/10.1007/s10470-022-02096-x.

5. S. Samanta and **S. Sarkar**, "A 10-bit CS-DAC using Fully Random Rotation based DEM and Code Independent Output Impedance Compensation," AEU – International Journal of Electronics and Communications, January, 2023, pp. 154528, doi: https://doi.org/10.1016/j.aeue.2023.154528.

6. **Santanu Sarkar** and Swapna Banerjee, "A 10- bit High-Performance DAC in 180-nm CMOS with high-FOM", Analog Integrated Circuits and Signal Processing, Springer, vol. 80, issue 1, July 2014, pp. 59-68. DOI: 10.1007/s10470-014-0309-x.

7. **Santanu Sarkar** and Swapna Banerjee, "An 8 bit Low Power DAC with Re-Used Distributed Binary Cells Architecture for Reconfigurable Transmitters", Microelectronics Journal, Elsevier, vol. 45, issue 6, June 2014, pp. 666-677. DOI: 10.1016/j.mejo.2014.03.014.

II. National and International Conference:

1. Deepika Kumaradasan, Sougata K Kar and Santanu Sarkar, "An 8-bit 100 kS/s Low Power SAR ADC with Modified EPC for Bio-Medical Applications", IEEE Silchar Subsection Conference (SILCON, November 3-5, 2023.

2. S. Samanta and S. Sarkar, "Dynamic Switching Compensation Technique Mitigating Code-Dependent Switching Distortion in CS-DACs,"2022 IEEE 19th India Council International Conference (INDICON), November, 2022.

3. Smrutilekha Samanta and Santanu Sarkar, "A 10-bit 500 MSPS Segmented CS-DAC of > 77 dB SFDR upto the Nyquist with Hexa-decal biasing", IEEE 24th International Symposium on VLSI Design and Test (VDAT), 23-25 Jul, 2020, IIT Bhubaneswar, Odisha. DOI:10.1109/VDAT50263.2020.9190402.

4. Smrutilekha Samanta and Santanu Sarkar, "A 1.8 V 8-bit 500 MSPS Segmented Current Steering DAC with > 66 dB SFDR", IEEE Computer Society Annual Symposium on VLSI (ISVLSI20), Jul 6-8, 2020, Limassol, CYPRUS. DOI:10.1109/ISVLSI49217.2020.00013.

5. Sachin Khandagale and Santanu Sarkar, "A 6-Bit 500 MSPS Segmented Current Steering DAC with On-Chip High Precision Current Reference," in IEEE International Conference on Computing, Communication and Automation (ICCCA2016), 29-April 2016. DOI: 10.1109/CCAA.2016.7813858.

6. Sachin Khandagale and Santanu Sarkar, "An 8-Bit 500 MSPS Segmented Current Steering DAC Using Chinese Abacus Technique," in 20th International Symposium on VLSI Design and Test (VDAT), 24-May 2016. **DOI:** 10.1109/ISVDAT.2016.8064903.

7. Santanu Sarkar and Swapna Banerjee, "A 10-bit 500 MSPS Segmented DAC with Distributed Octal Biasing Scheme", International Conference on Signal Processing, Computing and Control (ISPCC 15), Solan, Himachal Pradesh, India, 25-Sept 2015, pp. 145-148. DOI: 10.1109/ISPCC.2015.7375014.

8. Santanu Sarkar and Swapna Banerjee, "A 10-bit 500 MSPS Segmented DAC with Optimized Current Sources to Avoid Mismatch Effect", IEEE Computer Society Annual Symposium on VLSI (ISVLSI15), Montpellier, France, 09-July 2015, pp. 172-177. DOI: 10.1109/ISVLSI.2015.87.

9. Santanu Sarkar and Swapna Banerjee, "500 MHz Differential Latched Current Comparator for Calibration of Current Steering DAC", IEEE Student's Technology Symposium (IEEE TechSym), IIT Kharagpur, 28-Feb 2014, pp. 309-312. DOI: 10.1109/TechSym.2014.6808066.

10. Santanu Sarkar and Swapna Banerjee, "Design of SEU Tolerant Rad-Hard LVDS Driver for Space Applications", International Conference on VLSI and Signal Processing (ICVSP), E & ECE Dept., IIT Kharagpur, 10-Jan 2014, pp. 1-4.

11. Santanu Sarkar and Swapna Banerjee, "An 8-bit 1.8V 500 MSPS CMOS Segmented Current Steering DAC", Proceedings of IEEE Computer Society Annual Symposium on VLSI 2009 (ISVLSI), Tampa, Florida, 14-May, 2009, pp. 268-273. DOI: 10.1109/ISVLSI.2009.12.

12. Santanu Sarkar, R. S. Prasad, S. K. Dey, V. Belde and S. Banerjee, "An 8-bit, 1.8V, 500MS/s CMOS DAC with a Novel Four Stage Current Steering Architecture", IEEE International Symposium on Circuits and Systems (ISCAS), Seattle, Washington, USA, 19-May 2008, pp. 149-152. DOI: 10.1109/ISCAS.2008.4541376.

13. Santanu Sarkar, S. K. Dey, V. Belde and S. Banerjee, “A Novel and Simple, Supply Voltage and Temperature Compensated Current Reference”, Conference on Advances in Space Science and Technology (CASST), IIT Kharagpur, Jan 2008, pp. 1-3.

Patent Filed

1. A patent has been filed for the invention of "Realization of low mid-code glitch and high SFDR, Hybrid current steering DAC, reusing distributed binary cells".
   File no: 724/KOL/2013, India, Status: First Examination Report Submitted and Published.

Monogram Published

1. “Designing an 8-bit CMOS Low Glitch Digital-to-Analog Converter”
   Publisher: LAP LAMBERT, ISBN CODE: 978-3-8383-9082-6, Year-2010

CAD Skills

Programming Language and Design Tools: Cadence for analog circuit Design, Simulation and Layout (Schematic Composer, Analog Design Environment and Virtuoso Layout Editor), MatLab, Verilog, VHDL, Verilog-A.

List of Workshop Organized:

Sl.No.	Title	Sponsor	Amount	From Date (Month-Year)	To Date (Month-Year)	Mode of Workshop
1.	Micro-Sensors and Interfacing Circuits (MSIC-2022	SERB, Govt. of India	30,000/	18 July 2022	22 July 2022	Online
2.	Analog and Digital VLSI Design Flow and Embedded System Design	SERB, Karyashala-High End Workshop, Govt. of India	5 lakh	4 July 2022	13 July 2022	Physical mode (few Online candidates also)

List of Technology Developed/Demonstrated:

Sl.No.	Title	Year	Affiliated Institution	Brief Detail	References
1.	8-bit 100 MSPS Current Steering DAC	2009	IIT Kharagpur	Design and development of 8-bit digital-to-	Santanu Sarkar and Swapna Banerjee, “An 8 bit Low Power DAC with Re-Used

				analog converter for a sponsored project of SAC, ISRO.	Distributed Binary Cells Architecture for Reconfigurable Transmitters", Microelectronics Journal, Elsevier, vol. 45, issue 6, June 2014, pp. 666-677. DOI: 10.1016/j.mejo.2014.03.014.
2.	10-Bit 500 MSPS Current Steering DAC	2014	IIT Kharagpur	Design and development of 10-bit digital-to-analog converter for a sponsored project of SAC, ISRO.	Santanu Sarkar and Swapna Banerjee, "A 10- bit High-Performance DAC in 180-nm CMOS with high-FOM", Analog Integrated Circuits and Signal Processing, Springer, vol. 80, issue 1, July 2014, pp. 59-68. DOI: 10.1007/s10470-014-0309-x.
3.	6-Bit 100 MSPS Current Steering DAC	2022	NIT Rourkela	Design and development of 6-bit digital-to-analog converter in UMC 180 nm CMOS technology.	S. Samanta and S. Sarkar, "A Pairwise Swap Enabled Randomized DEM Addressing Intersegment Mismatch for Current Steering Digital-to-Analog Converters," in **IEEE Transactions on Very Large Scale Integration (VLSI) Systems**, vol. 30, no. 9, pp.1332-1340, Sept. 2022, doi: 10.1109/TVLSI.2022.3183353.
3.	Design of a 12-bit SAR ADC	2017	NUS, Singapore	Design and development of a 12-bit low power analog-to-digital converter in 40 nm CMOS technology in TSMC.	Karim Ali Ahmed, Jinq Horng Teo , Santanu Sarkar , Massimo Alioto, "Dual-Mode Conversion Gating, Comparator Merging and Reference-Less Calibration for 2.7X Energy Reduction in SAR ADCs under Low-Activity Inputs," IEEE Solid-State Circuits Letters, Feb 2023, doi: 10.1109/LSSC.2023.3246063.

Award & Achievements

1. Selected as TOP-9 designer in Cadence Design Contest, organized by Cadence Design Systems, India in the year 2008 for the design entitled "Design and On-chip Implementation

of an 8-bit Current Steering DAC with Low IBT-glitch for Digital Video and Telecommunication Applications".

2. Awarded National Scholarship in Secondary Examination.
3. IEEE Senior Member
4. Worked as a reviewer in several IEEE conferences, and for the following prestigious journals:
   a) IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
   b) IEEE Transactions on Microwave Theory and Techniques
   c) Microelectronics Journal, Elsevier
   d) Analog Integrated Circuits and Signal Processing, Springer
   e) Journal of Circuits, Systems and Computers.

Administrative Roles in Department and Institute

1. Faculty Advisor
2. Professor in Charge (PIC) of Circuits and Systems lab
3. Curriculum Development Committee member
4. Co-coordinator NSS
5. Departmental Training and Placement Coordinator
6. Departmental Information Committee member
7. Departmental Purchase Committee member